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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,271	03/10/2004	Glenn Algie	7000-248	2945

27820 7590 09/28/2009

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EXAMINER	
NGUYEN, ANH NGOC M	
ART UNIT	PAPER NUMBER
2416	
MAIL DATE	DELIVERY MODE
09/28/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/797,271	ALGIE ET AL.	
	Examiner	Art Unit	
	Anh Ngoc Nguyen	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 February 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Amendment

1. Applicants' Arguments/Remarks filed 06/03/2009 with respect to claims 1 – 20 have been fully considered but they are not persuasive.

Claims 1 – 20 are pending.

Response to Arguments

2. Examiner noted that claims 1 - 5 contain the claimed limitation of "adapted to" which make the steps/functions which follows "adapted to" to be performed are optional. Applicants' arguments that "adapted to" language is a positive limitation and must be considered when weighting patentability. Based on the above statement from Applicants and now of record, "adapted to" has been given patentable weight.

Claims 7 – 12 and 17 – 20 are rejected under 35 U.S.C. 101 as not falling within one of the four statutory categories of invention. While the claims recite a series of steps or acts to be performed, a statutory "process" under 35 U.S.C. 101 must (1) be tied to another statutory category (such as a particular apparatus), or (2) transform underlying subject matter (such as an article or material) to a different state or thing. The method of claims 7 – 12 and 17 – 20 are not performed by the apparatus therefore the rejection under 35 U.S.C. 101 is maintained.

Regarding Applicants' arguments on independent claims 1 and 7 with respect to limitations a), b), c) and i) to iii), please see responses of Final Rejection dated 08/18/2008 and Advisory Action dated 10/29/2008.

Applicants' allege that Chou et al. (US 7,043,569) do not teach or suggest the following:

"such that the applied interface personality provides an appropriate interconnection between the control system interface and the one of the plurality of module interfaces via a plurality of pins"

Examiner respectfully disagrees. Chou teaches values of one or more input pins of the interconnect device are used to identify such storage device. FIG. 6 illustrates an exemplary table 600 used to determine how to access a storage device storing configuration data associated with the interconnect device (see col. 8 lines 30 - 37). In one embodiment, each block of configuration data received from the non-volatile storage device includes information identifying a unit within the interconnect device that should receive this block of configuration data (see col. 7 lines 62 - 67). Figure 7 shows each configuration data block with its own destination Node ID and destination node address for identifying a unit within the interconnect device. The pins provide the interconnection for accessing the storage device that contains configuration data unit for distribution to the various unit located within the interconnect device. Referring to FIG. 6, column 602 stores values of the interconnect device's input pin which is designated to indicate whether the interconnect device is coupled to an independent NVRAM via an I2C bus. Column 604 stores values of the interconnect device's input pin which is designated to indicate whether the interconnect device is coupled to a processor subsystem (including an NVRAM) via a processor bus. Column 608 stores values of a control register bit at the processor bus. Column 608 indicates whether the NVRAM storing required information should be accessed via the I2C bus or the processor bus (see col. 8 lines 37 - 47).

As a result the argued features are shown by the cited references as follows:

DETAILED ACTION

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 7 – 12 and 17 – 20 are rejected under 35 U.S.C. 101 as not falling within one of the four statutory categories of invention. While the claims recite a series of steps or acts to be performed, a statutory "process" under 35 U.S.C. 101 must (1) be tied to another statutory category (such as a particular apparatus), or (2) transform underlying subject matter (such as an article or material) to a different state or thing (Reference the May 15, 2008 memorandum issued by Deputy Commissioner for Patent Examining Policy, John J. Love, titled "Clarification of 'Processes' under 35 U.S.C. 101"). The instant claims neither transform underlying subject matter nor positively tie to another statutory category that accomplishes the claimed method steps, and therefore do not qualify as a statutory process.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 – 12, 16 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chou et al (US 7,043,569) in view of Moon et al (US 7,000,052).

Chou discloses method and apparatus for configuring an interconnect device comprising the following features:

Regarding claim 1, Chou discloses an adaptive interconnect (see Fig. 2, col. 1 lines 40 - 55, col. 3 lines 4 – 25 and col. 4 lines 36 – 40, switch 200) for providing an interface between multiple modules and a control system comprising: a) a control system interface (see Fig. 3A, processor subsystem interface 304); b) a plurality of module interfaces (see col. 3 lines 20 – 25 and Fig. 2, PORTS 1 - 9); and c) adaptive interconnect logic (see col. 4 lines 1 – 14 and Fig. 2, management port 208) associated with the control system interface and the plurality of module interfaces (see Fig. 2 and Fig. 3A, management port is coupled to ports 1 – 9 and processor subsystem interface 304) and adapted to:

i) negotiate with a module over a control path (see Fig. 2, Fig. 3A – 3C, col. 3 lines 25 – 47, col. 4 lines 25 – 35 and col. 5 lines 15 - 48, competing requests for switch resources) via one of the plurality of module interfaces to identify an interface personality for the module (see Fig. 2, col. 5 lines 28 – 48 and col. 6 lines 64 – 67, identifying a storage device storing the configuration data and sending a request for the configuration data); ii) load the interface personality based on negotiations with the module (see Fig. 2, col. 3 lines 32 – 37 and col. 4 lines 40 - 45, loading the configuration data); and iii) apply the interface personality to the one of the plurality of module interfaces (see Fig. 3A – 3C, Fig. 4, Fig. 5, col. 2 lines 25 – 30, col. 4 lines 20 – 25, lines 42 – 46, col. 6 lines 20 – 28 and col. 8 lines 1 - 10, providing the configuration data to various components of switch 200),

such that the applied interface personality provides an appropriate interconnection between the control system interface (see Fig. 3A, processor subsystem interface 304) and the one of the plurality of module interfaces (see col. 3 lines 20 – 25 and Fig. 2, PORTS 1 - 9) via a plurality of pins (see Fig. 2, Fig. 5, Fig. 6, col. 8 lines 20 – 50, values of one or more input pins of the interconnect device are used to identify such storage device).

Regarding claims 2, Chou discloses wherein different interface personalities can be implemented simultaneously among the plurality of module interfaces (see col. 4 lines 20 – 25 lines 42 – 46 and col. 6 lines 20 – 28, providing the configuration data to units of the switch).

Regarding claims 3, Chou discloses wherein the adaptive interconnect logic is further adapted to renegotiate with the module over the control path if initial negotiations fail (see col. 4 lines 43 – 50, reloading the configuration information when resetting the interconnect device).

Regarding claim 4, Chou discloses wherein if the renegotiation fails, the adaptive interconnect logic is further adapted to send a notification of failure (see col. 3 lines 55 – 67, verify whether the POST has passed or failed).

Regarding claim 5, Chou discloses wherein the adaptive interconnect logic (see Fig. 2, management port 208) is further adapted to: a) receive a stimulus indicative of a change in personality for the module (see col. 5 lines 49 – 62, receiving an indicator); b) renegotiate with the module over the control path via the one of the plurality of module interfaces to identify a new interface personality for the module (see col. 4 lines 43 – 50, reloading the configuration information when resetting the interconnect device); c) load the new interface personality based on the renegotiations with the module (see col. 4 lines 40 – 42, loading configuration information); and d) apply the new interface personality to the one of the plurality of module

interfaces (see col. 4 lines 42 – 46 and col. 6 lines 20 – 28, providing the configuration data to units of the switch).

Regarding claim 7, Chou discloses a method for providing an interface between multiple modules and a control system comprising: a) negotiating with a module over a control path (see Fig. 2, Fig. 3A – 3C, col. 3 lines 25 – 47, col. 4 lines 25 – 35 and col. 5 lines 15 - 48, competing requests for switch resources) via one of a plurality of module interfaces to identify an interface personality for the module (see Fig. 2, col. 5 lines 28 – 48 and col. 6 lines 64 – 67, identifying a storage device storing the configuration data and sending a request for the configuration data);

b) loading the interface personality based on negotiations with the module (see Fig. 2, col. 3 lines 32 – 37 and col. 4 lines 40 - 45, loading the configuration data); and c) applying the interface personality to the one of the plurality of module interfaces (see Fig. 3A – 3C, Fig. 4, Fig. 5, col. 2 lines 25 – 30, col. 4 lines 20 – 25, lines 42 – 46, col. 6 lines 20 – 28 and col. 8 lines 1 - 10, providing the configuration data to various components of switch 200),

such that the applied interface personality provides an appropriate interconnection between the control system interface (see Fig. 3A, processor subsystem interface 304) and the one of the plurality of module interfaces (see col. 3 lines 20 – 25 and Fig. 2, PORTS 1 - 9) via a plurality of pins (see Fig. 2, Fig. 5, Fig. 6, col. 8 lines 20 – 50, values of one or more input pins of the interconnect device are used to identify such storage device).

Regarding claim 8, Chou discloses wherein different interface personalities can be implemented simultaneously among the plurality of module interfaces (see col. 4 lines 20 – 25 lines 42 – 46 and col. 6 lines 20 – 28, providing the configuration data to units of the switch).

Regarding claim 9, Chou discloses wherein the adaptive interconnect logic is further adapted to renegotiate with the module over the control path if initial negotiations fail (see col. 4 lines 43 – 50, reloading the configuration information when resetting the interconnect device).

Regarding claim 10, Chou discloses wherein if the renegotiation fails, the adaptive interconnect logic is further adapted to send a notification of failure (see col. 3 lines 55 – 67, verify whether the POST has passed or failed).

Regarding claim 11, Chou discloses wherein the adaptive interconnect logic (see Fig. 2, management port 208) is further adapted to: a) receive a stimulus indicative of a change in personality for the module (see col. 5 lines 49 – 62, receiving an indicator); b) renegotiate with the module over the control path via the one of the plurality of module interfaces to identify a new interface personality for the module (see col. 4 lines 43 – 50, reloading the configuration information when resetting the interconnect device); c) load the new interface personality based on the renegotiations with the module (see col. 4 lines 40 – 42, loading configuration information); and d) apply the new interface personality to the one of the plurality of module interfaces (see col. 4 lines 42 – 46 and col. 6 lines 20 – 28, providing the configuration data to units of the switch).

Chou discloses the claimed limitations as stated above. Chou does not specifically disclose the following features: regarding claims 1 and 7, selecting the interface personality; regarding claims 5 and 11, selecting the new interface personality; regarding claims 6 and 12, wherein negotiating, selecting and applying the interface personality are dynamic and occur automatically upon plugging the module into the one of the plurality of module interfaces; regarding claim 16, wherein the interface personality further defines an acceptable protocol for

communications with the module; regarding claim 20, wherein the interface personality further defines an acceptable protocol for communications with the module.

Moon discloses system and method for configuring and deploying I/O cards in a communications environment comprising the following features:

Regarding claims 1 and 7, Moon discloses selecting the interface personality (see abstract, col. 1 lines 50 – 55, a selected configuration parameter).

Regarding claims 5 and 11, Moon discloses selecting the new interface personality (see abstract and col. 1 lines 50 – 55, selected configuration).

Regarding claims 6 and 12, Moon discloses wherein negotiating, selecting and applying the interface personality are dynamic and occur automatically upon plugging the module into the one of the plurality of module interfaces (see col. 2 lines 4 – 15 lines 60 – 63, col. 3 lines 14 – 25, col. 6 lines 1 – 16, automatically configured resources and 'plug and play').

Regarding claim 16, Moon discloses wherein the interface personality further defines an acceptable protocol for communications with the module (see col. 2 lines 42 – 63, implemented in conjunction with any other suitable protocol according to particular needs).

Regarding claim 20, Moon discloses wherein the interface personality further defines an acceptable protocol for communications with the module (see col. 2 lines 42 – 63, implemented in conjunction with any other suitable protocol according to particular needs).

It would have been obvious to one ordinary skilled in the art at the time the invention was made to modify the invention of Chou, and use the features, as taught by Moon, thus providing for an efficient configuration and deployment technique, as discussed by Moon (see col. 1 lines 35 - 45).

7. Claims 13, 14, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chou et al (US 7,043,569) in view of Moon et al (US 7,000,052) and further in view of Moyer (5,689,714).

Chou and Moon disclose the claimed limitations as stated in paragraph 6 above.

Regarding claim 13, Chou discloses wherein the plurality of pins include data path pins (see col. Fig. 5, Fig. 6, col. 8 lines 30 - 50).

Regarding claim 17, Chou discloses wherein the plurality of pins include data path pins (see col. Fig. 5, Fig. 6, col. 8 lines 30 - 50).

Chou does not specifically disclose the following features: regarding claim 13, wherein the plurality of pins include power pins and control pins; regarding claim 17, wherein the plurality of pins include power pins and control pins.

Regarding claim 13, Moon discloses wherein the plurality of pins include power pins (see col. 5 lines 32 – 37 and col. 7 lines 45 - 56).

Regarding claim 17, Moon discloses wherein the plurality of pins include power pins (see col. 5 lines 32 – 37 and col. 7 lines 45 - 56).

It would have been obvious to one ordinary skilled in the art at the time the invention was made to modify the invention of Chou, and use the features, as taught by Moon, thus providing for an efficient configuration and deployment technique, as discussed by Moon (see col. 1 lines 35 - 45).

Chou and Moon do not specifically disclose the following features: regarding claim 13, wherein the plurality of pins include control pins; regarding claim 14, wherein the adaptive interconnect logic negotiates with the module using the control pins; regarding claim 17, wherein

the plurality of pins include control pins; regarding claim 18, wherein the negotiating step with the module is performed using the control pins.

Moyer discloses method and apparatus for providing low power control of peripheral devices using the register file of a microprocessor comprising the following features:

Regarding claim 13, Moyer discloses wherein the plurality of pins include control pins (see Fig. 1, control pins 32).

Regarding claim 14, Moyer discloses wherein the adaptive interconnect logic negotiates with the module using the control pins (see Fig. 1, Fig. 2, col. 2 lines 40 – 55 and col. 4 lines 1 - 25).

Regarding claim 17, Moyer discloses wherein the plurality of pins include control pins (see Fig. 1, control pins 32).

Regarding claim 18, Moyer discloses wherein the negotiating step with the module is performed using the control pins (see Fig. 1, Fig. 2, col. 2 lines 40 – 55 and col. 4 lines 1 - 25).

It would have been obvious to one ordinary skilled in the art at the time the invention was made to modify the invention of Chou and Moon, and have the features, as taught by Moyer, thus providing for a rapid status and control access between a peripheral device and the CPU of a microcontroller, as discussed by Moyer (see col. 1 lines 45 - 50).

8. Claims 15 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chou et al (US 7,043,569) in view of Moon et al (US 7,000,052) and further in view of Tzlil et al. (US 6,392,891).

Chou and Moon disclose the claimed limitations as stated in paragraph 6 above. Chou and Moon do not specifically disclose the following features: regarding claim 15, wherein the interface personality further defines signal levels for communications with the module; regarding claim 19, wherein the interface personality further defines signal levels for communications with the module.

Tzlil discloses utilizing a convection cooled electronic circuit card for producing a conduction cooled electronic card module comprising the following features:

Regarding claim 15, Tzlil discloses wherein the interface personality further defines signal levels for communications with the module (see col. 1 lines 23 - 35).

Regarding claim 19, Tzlil discloses wherein the interface personality further defines signal levels for communications with the module (see col. 1 lines 23 - 35).

It would have been obvious to one ordinary skilled in the art at the time the invention was made to modify the invention of Chou and Moon, and have the features, as taught by Tzlil, thus to utilize a standard convection cooled circuit card for the production of a novel conduction cooled circuit card module to improve conduction cooling, as discussed by Tzlil (see col. 2 lines 27 - 40).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Examiner's Note: Examiner has cited particular paragraphs, columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner. In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and, also to verify and ascertain the metes and bounds of the Claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Ngoc Nguyen whose telephone number is (571) 270-5139. The examiner can normally be reached on M - F, from 7AM to 3PM (alternate first Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kwang Yao can be reached on 5712723182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Anh Ngoc Nguyen/
Examiner, Art Unit 2416
09/25/2009

/Steven HD Nguyen/

Primary Examiner, Art Unit 2416